IN THE CLAIMS:

Applicants amended claims 12-14. No claims have been added or canceled. The listing of claims replaces all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Previously Presented) In a digital optical network, a method of buffering and reading path overhead bytes, comprising:

identifying a plurality of path overhead bytes as they are received;

selecting a subset of path overhead bytes from said plurality of path overhead bytes;

determining a signal number (S#) for each byte of said subset of path overhead bytes;

determining a path overhead number (P#) for each byte of said subset of path overhead bytes based on which one of said path overhead bytes is selected;

storing path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into a RAM FIFO buffer, wherein the RAM FIFO comprises a plurality of entries, each entry comprising a first section for storing a path overhead byte, a second section for storing a signal number (S#), and a third section for storing a path overhead number (P#); and

reading said entries from the RAM FIFO, wherein said entries are stored and read from the RAM FIFO in accordance with a first-in-first-out (FIFO) protocol.

2. (Original) The method of claim 1 further comprising:

incrementing a first counter each time one of said path overhead bytes is stored in one of said entries;

incrementing a second counter for each entry that is read;

determining when a difference in values between said first counter and said second counter reaches a specified value (N);

generating an interrupt signal when the difference reaches N;

transmitting the interrupt signal to a processor; and

initiating said step of reading when the interrupt signal is received by the processor.

3. (Original) The method of claim 1 further comprising:

incrementing a first counter each time one of said path overhead bytes is stored in one of said entries;

incrementing a second counter for each entry that is read;

periodically polling said first and second counters at specified time intervals to determine a difference in values between the first and second counters; and

initiating said step of reading when the difference reaches a specified value.

4. (Original) The method of claim 1 wherein said step of reading comprises burst mode reading of entries from said RAM FIFO.

5. (Original) The method of claim 1 wherein said step of reading comprises direct memory access (DMA) reading of entries from said RAM FIFO.

6. (Original) The method of claim 1 wherein said step of storing comprises storing only path overhead bytes meeting desired criteria, wherein said desired criteria includes any combination of said signal numbers (S#) and said path overhead numbers (P#).

7. (Previously Presented) In a digital optical network, a method of buffering and reading path overhead bytes, comprising:

identifying a plurality of path overhead bytes as they are received;

selecting one or more bytes of said plurality of path overhead bytes;

determining a signal number (S#) for each byte of said path overhead bytes selected;

determining a path overhead number (P#) for each byte of said path overhead bytes selected;

storing a first subset of said path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a first RAM FIFO buffer, wherein the first RAM FIFO includes a plurality of entries, each entry comprising a

first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third section for storing a respective path overhead number (P#), wherein said first subset of path overhead bytes have signal numbers corresponding to a first set of values;

storing a second subset of said path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a second RAM FIFO buffer, wherein the second RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third section for storing a respective path overhead number (P#), wherein said second subset of path overhead bytes have signal numbers corresponding to a second set of values; and

reading said entries from the first and second RAM FIFOs, wherein entries are stored and read from each respective first and second RAM FIFO in accordance with a first-in-first-out (FIFO) protocol.

8. (Original) The method of claim 7 wherein said step of reading comprises reading said first and second RAM FIFOs in parallel.

9. (Original) The method of claim 7 wherein said step of reading comprises burst mode reading said first and second RAM FIFOs in parallel.

10. (Original) The method of claim 7 wherein said step of reading comprises direct memory access (DMA) reading said first and second RAM FIFOs in parallel.

11. (Original) The method of claim 7 wherein said steps of storing comprise storing only path overhead bytes meeting desired criteria into said respective first and second RAM FIFOs, wherein said desired criteria includes any combination of said signal numbers (S#) and said path overhead numbers (P#).

12. (Currently Amended) An apparatus for buffering path overhead bytes, comprising:

a RAM FIFO buffer having a plurality of entries, each entry comprising a first section for storing a path overhead byte selected from a plurality of path overhead bytes for a synchronous payload envelope, a second section for storing a signal number (S#) and a third section for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored.

13. (Original) The apparatus of claim 12 wherein each entry of said plurality of entries comprises sixteen bits of storage capacity, said first section comprises eight bits of storage capacity, said second section comprises four bits of storage capacity, and said third section comprises four bits of storage capacity.

14. (Original) The apparatus of claim 12 further comprising:

a first counter that is incremented each time one of said path overhead bytes is stored in one of said entries; and

a second counter that is incremented for each of said entries that is read from said RAM FIFO.

15. (Previously Presented) An apparatus for buffering path overhead bytes, comprising:

a first RAM FIFO buffer having a first plurality of entries for storing a first set of path overhead bytes derived from a group of one or more bytes selected from a plurality of path overhead bytes for a synchronous payload envelope, wherein each of said first plurality of entries comprises a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored; and

a second RAM FIFO buffer having a second plurality of entries for storing a second set of path overhead bytes derived from one or more bytes of said plurality of path overhead bytes for said synchronous payload envelope, wherein each of said second plurality of entries comprises a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section

for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored, wherein said first set of path overhead bytes correspond to a first set of signal numbers and said second set of path overhead bytes correspond to a second set of signal numbers.

16. (Original) The apparatus of claim 15 wherein each entry of said first and second plurality of entries comprises sixteen bits of storage capacity, each of said first sections comprises eight bits of storage capacity, each of said second sections comprises four bits of storage capacity, and each of said third sections comprises four bits of storage capacity.

17. (Previously Presented) The apparatus of claim 15 further comprising:

a first counter that is incremented each time data an entry is stored in one of said first and second RAM FIFO; and

a second counter that is incremented for each entry that is read from said first and second RAM FIFOs.